Amendments to the Claims: This listing of claims will replace all prior versions, and listings, of claims in the application

Listing of Claims:

1. (Cancelled)

2. (Currently Amended) The [~~method~~] system of claim [~~1~~] 20 wherein the register is a memory mapped register.

3. (Currently Amended) The [~~method~~] system of claim [~~1~~] 20 wherein the register is an off-core register.

4. (Currently Amended) The [~~method~~] system of claim [~~1~~] 20 wherein [~~at least one of~~] the first and second processors are each [~~is~~] a digital signal processor (DSP).

5. (Cancelled)

6. (Cancelled)

7. (Cancelled)

8. (Currently Amended) The [~~method~~] system of claim 20 [~~1 including the steps of~~] wherein

[~~enabling~~] the register is enabled during a write cycle, and

[~~storing~~] the [~~parallel~~] bits of data are stored in the register when an address of the register matches a predetermined address.

9. (Currently Amended) A system for providing an interrupt signal from a first processor to a second processor comprising

a data bus coupled to the first processor for routing parallel bits of data,

a register and an edge detector both coupled between the first and second processors,

the [~~a~~] register coupled to the data bus for storing the parallel bits of data, at least one of the parallel bits of data having an active logic level,

the [~~an~~] edge detector coupled to the register for detecting active logic levels stored in the register and converting each active logic level into an interrupt signal, and

at least one line coupled between the edge detector and an interrupt terminal of the second processor for routing one of the interrupt signals to the interrupt terminal.

10. (Original) The system of claim 9 wherein the register includes a first set of flip/flops, each flip/flop storing one of the active logic levels, and

the edge detector includes a second set of flip/flops, each flip/flop detecting one of the active logic levels.

11. (Original) The system of claim 9 further including

an address bus coupled between the first processor and the register, and

a predetermined address for the register,

wherein the first processor routes the parallel bits of data to the register by setting the predetermined address on the address bus.

12. (Original) The system of claim 9 wherein the register is an off-core register and is enabled by a write strobe signal from the first processor.

13. (Original) The system of claim 9 wherein at least one of the first and second processors is a DSP.

14. (Currently Amended) In a multi-processor system having data lines between each processor and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register and a detector both coupled between the first and second processors,

the[~~a~~] register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

the[~~a~~] detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits from the detector to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

15. (Original) The system of claim 14 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

16. (Original) The system of claim 14 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

17. (Original) The system of claim 14 wherein at least one processor is a DSP.

18. (Original) The system of claim 14 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

19. (Original) The system of claim 14 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.

20. (Currently Amended) In an integrated circuit including at least two processors, data lines between each processor, and at least one interrupt terminal in each processor, a system for synchronizing a first processor with a second processor comprising

a register and a detector both coupled between the first and second processors,

the[~~a~~] register coupled to the data lines for storing data bits from the first processor, each data bit representing an interrupt signal,

the[a] detector for detecting each of the data bits in the register, and

a signal router for routing each of the detected data bits from the detector to a respective interrupt terminal in the second processor,

wherein when the first processor stores a data bit in the register, the router provides an interrupt signal to the second processor.

21. (Original) The system of claim 20 wherein the register includes a first set of flip/flops, each flip/flop storing one of the data bits, and

the detector includes a second set of flip/flops, each flip/flop detecting one of the data bits in the register.

22. (Original) The system of claim 20 wherein the signal router includes a set of lines, each line connected to the respective interrupt terminal.

23. (Original) The system of claim 20 wherein at least one processor is a DSP.

24. (Original) The system of claim 20 wherein at least one processor is a microprocessor.

25. (Original) The system of claim 20 further including an address bus coupled to the register, wherein the data bits are stored in the register when the first processor addresses the register.

26. (Original) The system of claim 20 wherein the data bits are stored in the register during a first clock cycle and the data bits are detected by the detector during a second clock cycle, and

the interrupt signal is enabled for a duration of a clock cycle.